P/N	Description
940-1819615	R@IC-PWM SOP-8 TH2267.1 Tape Melexis TH9384.2
940-1819615U	R@IC-PWM SOP-8 TH2267.1 UNTEST Tube-packed Melexis
940-1819615T	R@IC-PWM SOP-8 TH2267.1 Tube Melexis TH9384.2

Rev.	MR. Number	Date	Name

Freimaßtoleranzen
fein
mittel
grob
DIN

2004	Date	Name
Drawn	24.Dec	Joan. Shi
Approved	29/12	
Lfd -Nr		

FRIWO

Vendor P/N

Oberflache | EDV-Nr

Ausgangsteil

Description:
R@IC-PWM SOP-8 TH2267.1 Melexis

Scale

Part Number:
940-1819615X

inwards testing as per AQL /

Ersetzt

Melexis
Microelectronic Integrated Systems

Design specification of customer integrated circuit

TH2267.1

Version V2.2
Date 26.05.2004
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This document contains 12 pages.

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940-1819615X

Scale

1. Introduction

This document is based on the design specification „TH2267.1".

The valid specification for the ASIC development is the existing german version V2.2 from 26.02.2004. Functional modifications may occur during the design process, but must be agreed and signed off by both Melexis and customer.

1.1 Description

The TH2267 is an application specific device for the control of the primary side of a switched mode charger. The controlled variable is transferred by an additional winding from the secondary to the primary side. Additional references for the primary control function and the power supply are derived from the included bandgap reference. For control of the external bipolar transistor a push-pull driver stage is included. For the specific regulation characteristic resulting in driver switch-on and switch-off, current- and voltage monitoring with time constants and fixed characteristic curve are included. Overvoltage- and overcurrent-protection functions as well as voltage regulator and startup-circuit are included too. For the protection functions an additional z-diode reference contained.

1.2 Functional diagram (ASIC in application circuit)

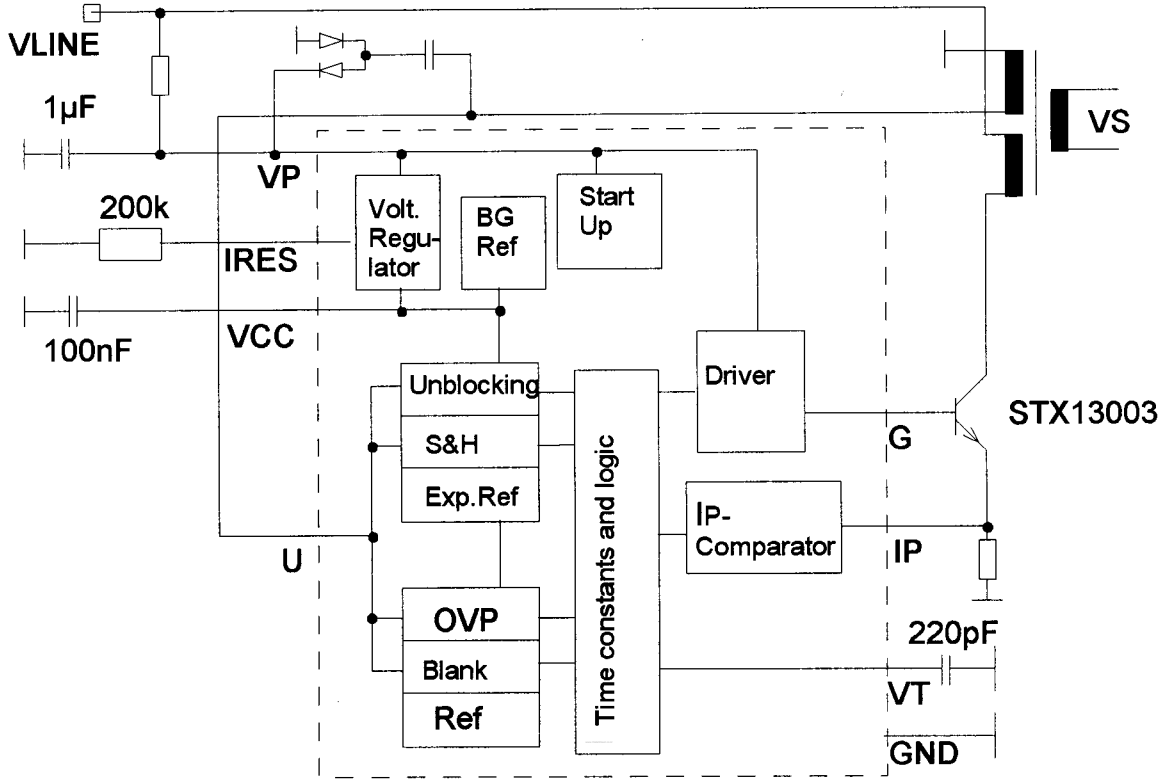

Figure 1: Functional diagram in principal application circuit

1.3 Hints on ESD/EMC

- The application circuit board should be designed to minimise electro-magnetic compatibility problems. ASIC can withstand disturbances smaller 40 V/m (< 2 GHz, <20 cm, Out < 0.5V). In this cases ASIC is in normal operating mode.
- The Chip is an ESD-sensitive device and should be handled according to guideline EN100015 part1 („The protection of ESD sensitive devices “).
- An ESD-robustness > 1000V according to MIL 883D is complied by the ASIC.

2. *Electrical characteristics*

All voltages are referenced to ground (GND = 0V).

Table 1 **Absolute maximum ratings**

NR.	Parameter	Symbol	Min	Max	Unit
1.0	IC Supply voltage	V_P	-0.3	45	V
		V_{CC}	-0.3	5.5	V
1.1	Input voltage, U	V_U	-45	50	V
1.2	Input voltage, other	V_{IN}	-0.3	V_{CC}+0.3	V
1.3	Output voltage	V_{OUT}	-0.3	V_{CC}+0.3	V
1.4	Input current	I_{IN}	-10	10	mA
1.5	Storage temperature	T_{STG}	-40	125	℃
1.6	Power dissipation	PD SOIC8		270	mW

Continuous operation of the device outside the defined "absolute ratings" is not allowed. It may cause permanent damage to the device. For the continuous operation of the device outside the defined "operating conditions" the correct function can not guaranteed. In this case the device reliability can be reduced.

Table 2 **Operating conditions**

NR.	Parameter	Symbol	Min	Typ	Max	Unit
2.0	IC Supply voltage	V_P	7.6 [1]		40 (44)[3]	V
			9.5 [2]		40 (44)[3]	V
2.1	Ambient temperature	T_A	-20		120	℃
2.2	Junction temperature	T_J			<=150	℃

[1] without voltage drop by driver switching

[2] with 100nF on Pin VP and 10µs power-on time of the driver; application circuit should be guaranteed, that the voltage at VP in case of driver switch-on not decrease under the undervoltage lockout threshold

[3] Continuous operation above 40V supply voltage violates the valid process specification of wafer supplier. This leads to degradation of reliability. This issue is more specified in chapter 8.

Table 3 **Static characteristics supply voltage, V_{CC}**
(V_p = 10V, T=-20 to 100 ℃)

NR.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
3.0	Supply Voltage	V_{CC}	C=100nF	4.5	5	5.5	V
3.1	Supply Current (average)	I_{IS}	before startup, T=25 ℃			85	µA
			before startup, T=100 ℃			130	µA
			static			440	µA
			dynamic [1], f_{CLK} <=100 kHz, without load			500	µA
3.2	Startup voltage	V_{STU}		15.0	20	22.5	V
3.3	Undervoltage (lockout)	V_{LO}		6	6.7	7.5	V

Table 4 **Static characteristics driver, pin G** (V_p = 10V, T = -20 to 100 ℃)
parameter 4.1 to 4.4 only measurable during reload time!

NR.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
4.0	Pull-down resistor	R_{PD}		13	19	25	kΩ
4.1	Output current source	$I_{SOURCEH}$	V_G = 2V	18	25	40	mA
4.2	Output current source after reload, $V_{IP} > V_{IP80\%}$	$I_{SOURCEL}$	V_G = 2V	0.3		1.5	mA
4.3	Output current sink	I_{SINK}	V_G > 2V	230		610	mA
4.4	Output voltage low	V_{GL}	I_{SINK}=30mA	0		0.2	V
4.5	Output voltage during startup and after lockout	V_{GSULO}				0.2	V

Table 5 **Static characteristics driver, pin IP**
(V_p = 10V, T = -20 to 100 ℃)

NR.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
5.0	Input current IP[1]	I_{IP}				0.5	µA
5.1	Threshold IP comparator	V_{IP}		435	485	535	mV
5.2	Threshold 80% IP comp.	$V_{IP80\%}$		345	395	455	mV

[1] Parameter only measured and documented during characterisation period of the IC. This test is not provided in production.

Table 6 **Static characteristics pin U** (V_p = 10V, T = -20 to 100 °C)

NR.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
6.0	Threshold enable comparator	V_{FREIG}		50	100	140	mV
6.1	Threshold OVP comparator	V_{OVP}		7.3	8.0	9.0	V
6.2	Threshold blank comparator	V_{AUSB}		-1.2	-1	-0.8	V
6.3	S&H reference	$V_{S\&HREF}$		3.9	4.2	4.6	V
6.4	S&H range[1]	$V_{S\&Hhub}$			±0.1		V
6.5	Input resistance[1]	R_U	dynamic	20	40	60	kΩ

Table 7 **Dynamic characteristics** (V_p = 10V, T = -20 to 100 °C, IRES = 200k)

NR.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
7.0	Lockout time [1]	T_{LO}	VG < 1V			1	µs
7.1	Minimal switch-on time	T_{LEB}		200	530	800	ns
7.2	IP delay (after T_{LEB}) [1]	T_{IP}	$V_{IP}=V_{IP}+50mV$, V_G< 1V,			100	ns
7.3	Minimal pause	$T_{PAUSEmin}$		1.0		2.8	µs
7.4	Maximal pause	$T_{PAUSEmax}$	U > $V_{S\&HREF}$ + 0.2V	3.5	4.2	7.3	ms
7.5	Blanking-time after OVP or fade-out	T_{OVP}		11	19	30	ms
7.6	Enable delay for fade-out	T_{AUSB}		200	530	800	ns
7.7	Short pulse suppression on AUSB [2]	T_{KAUSB}		60	180	280	ns
7.8	Current flow ratio[3]	T_{IREG}		51		60	%

[1] Parameter only measured and documented during characterisation period of the IC. This test is not provided in production.

[2] Parameter indirectly measured via T_{AUSB} + T_{KAUSB}.

3. *Timing-Diagrams*

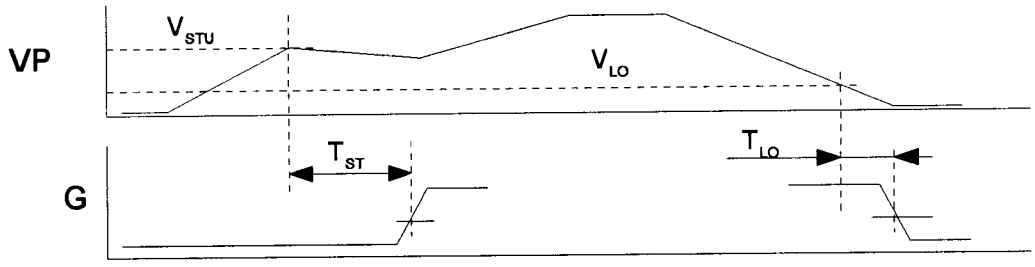

Figure 2: Startup and lockout time

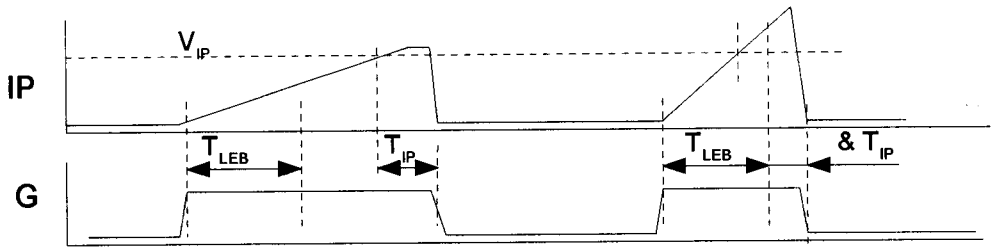

Figure 3: Switch-off through IP, after T_{LEB} and within T_{LEB}

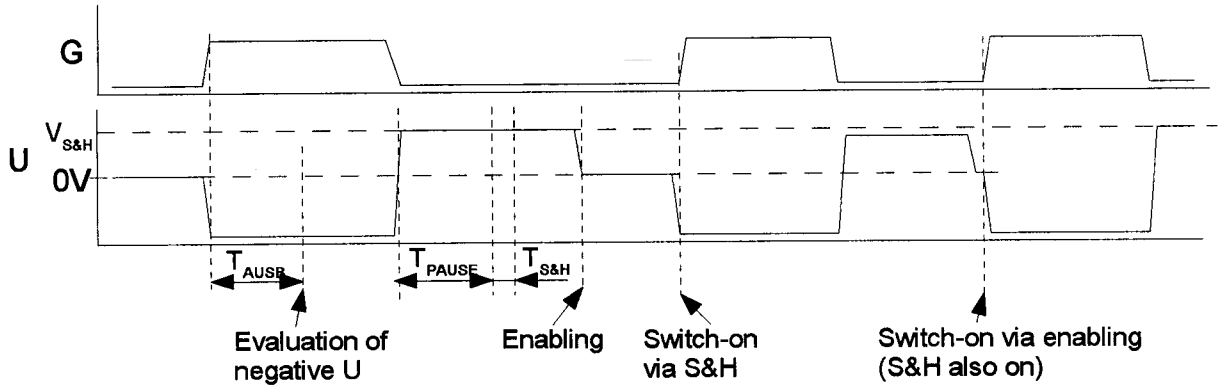

Figure 4: Normal function with switch-on per S&H or enabling

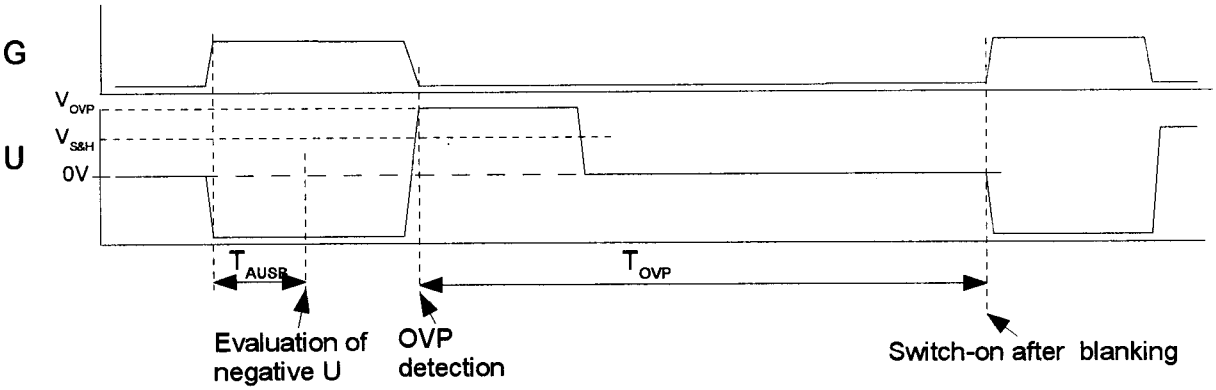

Figure 5: Activate of blanking time per OVP

4. Functional description

4.1 Functional flow

The TH2267 is a primary control unit for switch mode charger. The controlled variable is transferred by an auxiliary winding from the secondary to the primary side.

To activate the IC and switch-on the output driver, the IC supply voltage has to ramp up to the startup voltage. Exceeding the threshold voltage V_{IP}(represent the current of the primary coil via shunt measurement), the driver switch off. After 2/3 of the secondary current flow time (definite by enable), the voltage on the additional winding of the transformer stored by the sample and hold circuit. After compare of S&H-voltage with the exponential rising reference, the driver switch-on again and switch off at the threshold voltage V_{IP}. These toggle-behaviour persists as long as the IC supply voltage VP drops under the lockout voltage. Then the ASIC is deactivated.

In order to prevent undesirable operating conditions additional protection circuits are included. The energy transfer of the transformer is monitored by the enable-comparator (the voltage at the auxiliary winding < V_{FREIG}). An earlier switch-on of the driver is impossible. In case of high voltages (peaks) at the auxiliary winding (over the control range), the OVP-comparator switch-off the output for a definite blanking time. The negative voltage at the auxiliary winding in case of activated driver is monitored by the blanking-comparator.

Before startup the power supply of the AISC results directly from the line voltage. In operating mode the power supply is delivered from the auxiliary winding.

4.2 Driver

The driver is a push pull stage with the supply voltage V_p. He provides the driving power for the external bipolar transistor. The output signal is current-limited to I_{SOURCE}. The output is connected to ground by a pull-down resistor, due to a definite startup- and lockout-output impedance. Apart from startup sequence the driver is low ohmic and forces the output voltage to a low level. The reload time for high is determined by the static threshold $V_{IP80\%}$.

4.3 Startup and internal power supply

The voltage regulator provides the internal power supply V_{CC}. For the supply voltages V_{CC} and V_p external capacitors are required. The current biasing of the IC is adjustable by an external resistor. Internal time constants, thresholds and the output current depends from the value of this resistor.
The startup circuit activate the IC after startup and deactivate the IC in case of undervoltage lockout.

4.4 S&H-circuit and exponential reference

The regulation function is realised by transfer of the secondary voltage to the auxiliary

winding during the phase of interlock. The secondary voltage is defined by the transmission ratio between the secondary and auxiliary winding. The voltage at the auxiliary winding is located in adjustment range by the control of switching pauses. The information is only present during the phase of interlock. Therefore a sample and hold circuit holds the voltage level for the phase of energy flow and pause. The suppression of overshoot voltages after toggling of the external FET is realised by a time constant $T_{PAUSEmin}$. The sampling takes place after $T_{PAUSEmin}$. The S&H-voltage represent the amplified control deviation. Using the exponential reference these value transferred to a time-dependent value. A negative control deviation (lower voltage) generates short switch-off phases, positive (higher voltage) long switch-off phases. The maximum pause is limited to $T_{PAUSEmax}$. The replication of the load ratio is empathised by the exponential distribution of the reference. The aperture time for the acquisition of the actual value to the hold-capacitor is dependent from the time of secondary current flow. These time of current flow is stored as an integrated voltage value. The stored value define the sampling time for the following pulse by a ratio of 2/3.

4.5 IP comparator

The current trough the external bipolar transistor is monitored by the IP comparator. Above the IP-threshold (V_{IP}) the output is switched off. If the $V_{IP80\%}$ -threshold voltage at pin IP is reached, the driver switch to a high ohmic state. This function is suppressed for the minimum switch-on time t_{LEB} after switch-on of external power transistor.

4.6 Safety functions

Three additional comparators connected to pin U to prevent from undesirable operating conditions.
If the voltage at the auxiliary winding is zero (energy in the transformer is zero), the enable-comparator approve a switch-on of the driver. The comparator detect the time of secondary current flow.
Positive voltages above the adjustment range are monitored by the OVP-comparator. To prevent from overvoltages he forces the driver to switch-off for the blanking time. For suppression of overshoot voltages the comparator input is shielded by a 6-stepped rc-filter.
Negative voltages during switch-on time of the external power transistor are monitored by the blanking-comparator. In case of absent negative voltages he also triggered the blanking time for the driver to prevent from a defect connection IC <-> auxiliary winding. To prevent from trigger fails delay and short pulse suppression are included for this function.
OVP- and blanking-comparator are separated from enable and S&H connected to pin U .

5. Pin location and description

Pad	Pin SOIC8	Name	IO-type	Function
1	1	IP	I	current sense
2	2	IRES	I/O	bias resistor
3	3	VP	P	IC supply voltage
4	4	G	O	driver output
5	5	GND	P	ground
6	6	U	I	input for auxiliary winding
7	7	VCC	P	supply voltage
8	8	VT	I/O	external capacitor for current control

6. Package outlines

Engineering samples: CDIP8

Production: TH2267 SOIC8

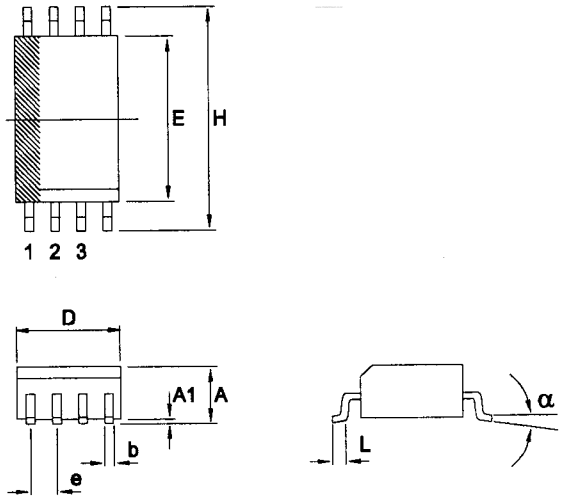

Figure 8: package SOIC8

6.1 Dimensions

Dim.		D	E	H	A	A1	e	B	L	Copl	α
mm	min	4.80	3.80	5.80	1.35	0.10	1.27	0.33	0.40		0°
	max.	5.00	4.00	6.20	1.75	0.25		0.51	1.27	0.10	8°
inch	min	0.189	0.150	0.228	0.053	0.004	0.050	0.013	0.016		0°
	max.	0.197	0.157	0.244	0.069	0.010		0.020	0.050	0.04	8°

7. Soldering

This Melexis device TH2267, SOIC8NB, Assembly Subcontractor Carsem, is classified and qualified regarding JEDEC020 and moisture sensitivity level 1 (MSL1) for a lead free soldering technology with a maximum peak temperature of 250℃.

Following test methods are applied:

- IPC/JEDEC J-STD-020

  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices

- MIL 883 Method 2003 / EIA/JEDEC JESD22-B102

  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc.) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a Roadmap to qualify their package families for lead free processes also. Various lead free generic qualifications are running, current results on request.

For more information on Melexis lead free statement see quality page at our website:
http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf

8. Higher supply voltage

The operation of the IC at higher supply voltages V_p >40V up to 44V is equivalent to higher stress for the device. According to the valid process specification of the wafer supplier the maximum IC voltage is 40V. Minimisation of the higher risk was investigated by Melexis. Results of the analysis are committed by report to Friwo (14.10.2003).

However, based on the results of the report there is to ascertain that a risk of (process-) failures exist (breakdown voltage < 50V). Averaged there is a smallish risk, but it's possible that single lots are not usable regarding to the higher supply voltage requirements. Because of the valid process specification, Melexis cannot accept the costs for these lots.
Therefor the following procedure is valid:

- In addition to the existing PCM-selection parameter UBPHV≥45V an additional PCM-selection parameter UBPHV≥50V established (each wafer measured).
- Friwo received an information in case of non-compliance to the additional selection criteria UBPHV≥50V.

- Friwo has to pay for these produced wafers after accounting.
- Melexis scraps the accrued wafers.

9. Specification history

Version	Date	Kind of change
1.1	25.10.02	parameter 1.6, 2.0, 4.1, 4.3 changed, parameter 7.9 added
1.2	2/17/2003	parameter 3.1, 3.2, 4.1, 4.2, 4.3, 5.1, 5.2, 6.0, 6.1, 6.3, 6.4, 7.1, 7.3, 7.4, 7.5, 7.6, 7.7, 7.8 regarding ppk-measurements from TH9384.2 modified, parameter 7.9 removed, parameter 6.0 adjusted
1.3	4/02/2003	tbd.-parameter fixed after ppk- measurements from TH9384.21
2.0	4/28/2003	parameter 4.1, 4.2, 4.3, 5.1, 5.2, 6.0, 6.1, 6.3, 7.1, 7.3, 7.4,7.5, 7.6, 7.7 regarding cpk-measurements from TH2267.1 modified
2.1	5/07/2003	Figure 1.2: 200k-resistor instead of 240k; parameter 3.1, 4.1, 4.2, 7.7 regarding cpk-measurements from TH2267.1 with 200k-reference resistor modified
2.2	2/26/2004	parameter 2.0 higher supply voltage, parameter 5.0 changed, chapter 7 edited, chapter 8 added